CLAIMS

1. An electrostatic discharge (ESD) protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential (VCC) and a second potential bus with a second supply potential (VSS), said electrostatic discharge protective structure comprising:

a laterally formed electrostatic discharge diode having a first region doped with a first conduction type and a second region, spaced apart from said first region;

a doped second conduction type, wherein said electrostatic discharge protective structure is located between the first and second potential busses and drains off an overvoltage pulse to one fo the first and second potential busses, wherein said laterally formed electrostatic discharge diode includes a gate electrode located between said first region and said second region corresponding to the width (W) or the length of the gate electrode.

2. The electrostatic discharge protective structure of claim 1, wherein said protective structure includes a semiconductor body having a surface in which said first region and said second region are embedded, wherein said first region is connected via a first electrode to the first potential bus, and said second region is connected via a second electrode to the second potential bus.

3. The electrostatic discharge protective structure of claim 2, wherein said semiconductor body includes charge carriers of the second conduction type, and said gate

electrode and said second electrode are connected to said second potential bus.

4. The electrostatic discharge protective structure of claim 2, wherein said semiconductor body includes charge carriers of the first conduction type, and at least one well of the second conduction type is embedded in said semiconductor body, and said first and second regions are embedded in said well.

5. The electrostatic discharge protective structure of claim 4, wherein said second regions laterally enclose said first regions.

6. The electrostatic discharge protective structure of claim 4, wherein the integrated semiconductor circuit is configured and arranged as an MOS or CMOS circuit.

7. The electrostatic discharge protective structure of claim 2, comprising a gate dielectric that spaces said semiconductor body at a distance from the gate electrode.

8. The electrostatic discharge protective structure of claim 7, wherein said gate dielectric contains silicon dioxide and said gate electrode contains polysilicon.

9. A method for producing an electrostatic discharge protective structure that is co-integrated into an integrated circuit with a circuit to be protected, and the electrostatic discharge protective circuit and the circuit to be protected are disposed electrically in parallel between first and second voltage busses, said method comprising:

inserting doping atoms of a first conduction type for the first region;

inserting doping atoms of a second conduction type for the second region;

applying a gate dielectric to the first surface over an enrichment region that is located between the first region and the second region;

applying a metallization or a polysilicon layer respectively to the first and second regions and to the gate dielectric.

10. The method of claim 9, wherein said gate dielectric and said gate electrode are produced first, and then said first and the second regions are inserted in a self-adjusting manner into the semiconductor body using the gate dielectric as a mask.

11. The method of claim 10, wherein said step of inserting doping atoms of a first conduction type for the first region includes the step of ion implantation of the doping atoms into the first region.

12. The method of claim 10, wherein said integrated semiconductor circuit and said electrostatic diode are produced in MOS/CMOS technology.

13. An integrated circuit with electrostatic discharge protection, said integrated circuit comprising:

a circuit to be protected;

an electrostatic discharge device that is disposed electrically parallel to said circuit to be protected between first and second voltage busses, wherein said electrostatic discharge device includes a laterally shaped electrostatic discharge diode having:

(i) a first region doped with a first conduction type material within a

substrate;

(ii) a second region doped with a second conduction type material within said substrate; and

(iii) a gate electrode having a width W and located between said first and second regions such that said first and second regions are separated by the width W.

14. The integrated circuit of claim 13, comprising a gate oxide disposed on said substrate between said first and second conduction regions and underlying said gate electrode.

15. The integrated circuit of claim 14, comprising a first electrode disposed on said substrate overlaying said first region, and a second electrode disposed on said substrate overlaying said second region, wherein said first electrode is connected to the first voltage bus and said second electrode is connected to said second bus.